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㊹発明の名称　半導体装置の製造方法

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明　細　書

1. 発明の名称

半導体装置の製造方法

2. 特許請求の範囲

1) (a) 絶縁性非晶質材料上にシリコンを主体とする非晶質材料層を形成する工程、

(b) 該非晶質材料層上に金属層を形成しパターン形成する工程、

(c) 熱処理等により、該非晶質材料層と該金属層が接触している領域に結晶核を生成させる工程、

(d) 該非晶質材料層を前記結晶核をシードとして、熱処理等により結晶成長させる工程、

(e) 結晶成長させたシリコン層に半導体素子を形成する工程を少なくとも有することを特徴とする半導体装置の製造方法。

3. 発明の詳細な説明

(産業上の利用分野)

本発明は、半導体装置の製造方法に係わり、特に、絶縁性非晶質材料上に選択的に結晶半導体層を形成する半導体装置の製造方法に関する。

(従来の技術)

ガラス、石英等の絶縁性非晶質基板や、SiO₂等の絶縁性非晶質膜上に、高性能な半導体素子を形成する試みが成されている。

近年、大型で高解像度の液晶表示パネルや、高速で高解像度の密着型イメージセンサや三次元IC等へのニーズが高まるにつれて、上述のような絶縁性非晶質材料上の高性能な半導体素子の実現が待望されている。

絶縁性非晶質材料上に薄膜トランジスタ(TFT)を形成する場合を例にとると、(1)プラズマCVD法等により形成した非晶質シリコンを素子材としたTFT、(2)CVD法等で形成した多結晶シリコンを素子材としたTFT、(3)超微細結晶化法等により形成した単結晶シリコンを素子材としたTFT等が検討されている。

ところが、これらのＴＦＴのうち非晶質シリコンもしくは多結晶シリコンを素子材としたＴＦＴは、単結晶シリコンを素子材とした場合に比べてＴＦＴの電界効果移動度が大幅に低く（非晶質シリコンＴＦＴ＜１ｃｍ²／Ｖ・ｓｅｃ、多結晶シリコンＴＦＴ～１０ｃｍ²／Ｖ・ｓｅｃ）、高性能なＴＦＴの実現は困難であった。

一方、レーザビーム等による溶融再結晶化法は、未だに十分に完成した技術とは言えず、また、液晶表示パネルの様に、大面積に素子を形成する必要がある場合には技術的困難が特に大きい。

そこで、絶縁性非晶質材料上に高性能な半導体素子を形成する簡便かつ実用的な方法として、大粒径の多結晶シリコンを固相成長させる方法が注目され、研究が進められている。（Thin Solid Films 100 (1983) p.237, JJAP Vol.25 No.2 (1986) p.L121）

〔発明が解決しようとする課題〕

しかし、従来の技術では、多結晶シリコンの粒径、結晶粒界の存在する位置を十分に制御することが困難であった。従って、仮に大粒径の多結晶シリコンが形成できたとしても、結晶粒の内部に形成されたＴＦＴと結晶粒界部にＴＦＴのチャンネル領域が位置したＴＦＴの間で特性が大幅に異なることから、ＴＦＴで構成した集積回路の動作速度が、結晶粒界部に位置する特性の悪いＴＦＴの特性で制限されたり、最悪の場合は、回路が動作しない等の重大な問題が発生した。

そこで、本発明は結晶粒界の位置を制御し、半導体素子を結晶領域に選択的に形成する製造方法を提供するものである。

〔課題を解決するための手段〕

本発明の半導体装置の製造方法は、

（ａ）絶縁性非晶質材料上にシリコンを主体とする非晶質材料層を形成する工程、

（ｂ）該非晶質材料層上に金属層を形成しパターン形成する工程、

（ｃ）熱処理等により、該非晶質材料層と該金属層が接触している領域に結晶核を生成させる工程、

（ｄ）該非晶質材料層を前記結晶核をシードとして、熱処理等により結晶成長させる工程、

（ｅ）結晶成長させたシリコン層に半導体素子を形成する工程を少なくとも有することを特徴とする。

〔実施例〕

第１図は、本発明の実施例における半導体装置の製造工程図の一例である。尚、第１図では半導体素子として薄膜トランジスタ（ＴＦＴ）を形成する場合を例としている。

第１図において、（Ａ）は、ガラス、石英等の絶縁性非晶質基板、もしくはＳｉＯ₂等の絶縁性非晶質材料層等の絶縁性非晶質材料１０１上にシリコンを主体とする非晶質材料層１０２を形成する工程である。該非晶質材料層の形成方法としては、プラズマＣＶＤ法、蒸着法、ＥＢ蒸着法、ＭＢＥ法、スパック法、ＣＶＤ法等で非晶質シリコンを成膜する方法と、微結晶シリコンもしくは多結晶シリコン等をプラズマＣＶＤ法、ＣＶＤ法、蒸着法、ＥＢ蒸着法、ＭＢＥ法、スパック法等で形成後、Ｓｉ、Ａｒ、Ｂ、Ｐ、Ｈｅ、Ｎｅ、Ｋｒ、Ｈ等の元素をイオン打ち込みして、該層結晶シリコンもしくは多結晶シリコン等を非晶質化する等の方法がある。

（Ｂ）は、該非晶質材料層１０２上に金属層１０３を形成し該金属層をシード領域１０４となる部分を残して除去し、熱処理等によって、該非晶質材料層１０２と金属層１０３が接触している部分にシードとなる結晶核を生成させる工程である。金属層としてＡｌを用いた場合を例にすると、該金属層１０３と接触している非晶質シリコンは他の部分と比べてより低温でしかも短時間で結晶核が発生し易い。そこで、金属層と接触していない部分からは結晶核が発生しない温度及び時間で熱処理を行うと、シード領域１０４から選択的に結晶成長を誘起することができる。具体的には、蒸着法等でＡｌを形成しパターン形成した後で、２００℃～４５０℃程度で１５分～２時間程度の熱処理を行うと、金属層と非晶質シリコン層

の界面付近には結晶核が生成し結晶成長が始まる。続いて、金属層（Ａｌ）１０３をリン酸等でエッチング除去する。金属層を除去する理由は、続いて行うより高い温度での熱処理の際、金属の非晶質シリコン中（特に素子形成領域まで）への異常拡散を防止するためである。又、Ａｌ等の金属層の膜厚を非晶質シリコン層の膜厚と比べて少なくとも同程度以下にすることも、上述の異常拡散を防止する対策となる。例えば、非晶質シリコン層２００Ａ～１０００Ａに対して、金属層１００Ａ～５００Ａ程度かこれよりも薄い金属層を用いたほうが異常拡散が低減される。

前、結晶核が生成する熱処理温度は非晶質シリコンの成膜方法によって最適値が異なる。例えば、プラズマＣＶＤ法で形成した非晶質シリコンの場合は２００℃～３５０℃程度の比較的低温で結晶核が形成される。そのため、シード領域以外から結晶核が生成されにくい低温の熱処理でシード領域に結晶核を生成できるメリットがある。

（Ｃ）は、該非晶質材料層１０２を該シード領域１０４を起点として、熱処理等により選択的に結晶成長させる工程である。熱処理温度は５５０℃～６５０℃程度で２０時間～３０時間程度の熱処理を行う。

（Ｄ）は、結晶成長させたシリコン層１０５に半導体素子を形成する工程である。尚、第１図（Ｄ）では、半導体素子としてＴＦＴを形成する場合を例としている。図において、１０６はゲート電極、１０７はソース・ドレイン領域、１０８はゲート絶縁膜、１０９は層間絶縁膜、１１０はコンタクト穴、１１１は配線を示す。ＴＦＴ形成法の一例としては、シリコン層１０５をパターン形成し、ゲート絶縁膜を形成する。該ゲート絶縁膜は熱酸化法で形成する方法（高温プロセス）とＣＶＤ法もしくはプラズマＣＶＤ法等で６００℃程度以下の低温で形成する方法（低温プロセス）がある。低温プロセスでは、基板として安価なガラス基板を使用できるため、大型な液晶表示パネルや密着型イメージセンサ等の半導体装置を低コストで作成できるほか、三次元ＩＣ等を形成する場合においても、下層部の素子に悪影響（例えば、不純物の拡散等）を与えずに、上層部に半導体素子を形成することが出来る。続いて、ゲート電極を形成後、ソース・ドレイン領域をイオン注入法、熱拡散法、プラズマドーピング法等で形成し、層間絶縁膜をＣＶＤ法、スパッタ法、プラズマＣＶＤ法等で形成する。さらに、該層間絶縁膜にコンタクト穴を開け、配線を形成することでＴＦＴが形成される。

本発明に基づく半導体装置の製造方法で作製した低温プロセスＴＦＴ（Ｎチャンネル）の電界効果移動度は、２００～３５０cm^2／Ｖ・ｓｅｃであり、ガラス基板上に高性能なＴＦＴを形成することが出来た。これは、本発明の製造方法により、選択的な結晶成長が再現性良くできるようになったほか可能となった。さらに、前記ＴＦＴ製造工程に水素ガスもしくはアンモニアガスを少なくとも含む気体のプラズマ雰囲気に半導体素子をさらす工程を設けると、欠陥密度が低減され、前記電界効果移動度はさらに向上する。

第２図及び第３図は、本発明の実施例における半導体装置の製造工程図の別の一例である。第２図は断面図、第３図は平面図である。

第２図及び第３図において、（Ａ）は、ガラス、石英等の絶縁性非晶質基板、もしくはＳｉＯ，等の絶縁性非晶質材料層等の絶縁性非晶質材料層２０１上にシリコンを主体とする非晶質材料層２０２を形成する工程である。該非晶質材料層の形成方法としては、プラズマＣＶＤ法、減圧法、ＥＢ蒸着法、ＭＢＥ法、スパック法、ＣＶＤ法等で非晶質シリコンを成膜する方法と、同結晶シリコンもしくは多結晶シリコン等をプラズマＣＶＤ法、ＣＶＤ法、減圧法、ＥＢ蒸着法、ＭＢＥ法、スパック法等で形成後、Ｓｉ、Ａｒ、Ｂ、Ｆ、Ｈｅ、Ｎｅ、Ｋｒ、Ｈ等の元素をイオン打ち込みして、該同結晶シリコンもしくは多結晶シリコン等を非晶質化する等の方法がある。

（Ｂ）は、該非晶質材料層２０２上に金属層２０３を形成し該金属層をシード領域２０４となる部分を残して除去し、熱処理等によって、金属層

２０３と該非晶質材料層２０２が接触している部分にシードとなる結晶核を生成させ、続いて、該非晶質材料層２０２を所定の形状にパターン形成する工程である。尚、シード領域を結晶化させる前に非晶質材料層のパターン形成を行ってもよい。金属層としてＡｌを用いた場合を例にすると、前述の通り該金属層２０３と接触している非晶質シリコンは他の部分と比べてより低温でしかも短時間で結晶核が発生し易い。そこで、金属層と接触していない部分からは結晶核が発生しない温度及び時間の熱処理を行うと、シード領域から選択的に結晶成長を誘起することができる。具体的には温度２００℃～４５０℃程度で１５分～２時間程度の熱処理を行うと、金属層と非晶質シリコン層の界面付近に結晶核が生成し結晶成長が始まる。続いて、金属層（Ａｌ）２０３をリン酸等でエッチング除去する。金属層を除去する理由は、前述の通り続いて行うより高い温度での熱処理の際、金属の非晶質シリコン中（特に素子形成領域まで）への異常拡散を防止するためである。

尚、結晶核が発生する熱処理温度は非晶質シリコンの成膜方法によって最適値が異なる。例えば、プラズマＣＶＤ法で形成した非晶質シリコンの場合は２００℃～３５０℃程度の比較的低温で結晶核が形成される。そのため、シード領域以外から結晶核が生成されにくい低温の熱処理でシード領域に結晶核を生成できるメリットがある。

続いて、非晶質シリコン層を所定の形状にパターン形成する。第２図では該非晶質シリコン層を素子を形成する領域となる島状領域２０５と該島状領域２０５と該シード領域２０４を結ぶ連結領域２０６を少なくとも有する形状にパターン形成する場合を例としている。

（Ｃ）は、該非晶質材料層２０２を該シード領域２０４を起点として、熱処理等により選択的に結晶成長させる工程である。熱処理温度は５５０℃～６５０℃程度で２０時間～３０時間程度の熱処理を行う。

非晶質シリコン層を前述の如く島状領域２０５と連結領域２０６を有する形状にパターン形成しておくと、シード領域で複数の結晶核が生成した場合でも、どちらか一方の優勢な（結晶成長速度が速い、又は、結晶核が早く発生した方の）結晶成長が速い連結領域で選択され、島状領域は単結晶化される。第４図にその結晶成長の模式図を示す。第４図において、４０１は島状領域、４０２は連結領域、４０３はシード領域、４０４及び４０５は結晶核を示す。

又、連結領域で唯一の結晶成長に選択されない場合でも第５図の結晶成長の模式図に示すように結晶粒界が存在する確立は大幅に減少される。第５図において、５０１は島状領域、５０２は連結領域、５０３はシード領域、５０４は結晶粒界が存在する確立が高い位置であり、５０５は結晶粒界の存在する確立がほぼ零の領域である。５０６は両者の中間の領域（グレーゾーン）である。従って、半導体素子として、ＭＯＳ型トランジスタやＴＦＴを例とするならば、該素子のチャンネル領域が領域４０５に入るように素子を配置すれば、結晶粒界による素子特性の大幅なばらつきを抑くすことができる。

（Ｄ）は、結晶成長させた島状領域２０５に半導体素子を形成する工程である。尚、第２図（Ｄ）では、半導体素子としてＴＦＴを形成する場合を例としている。図において、２０７はゲート電極、２０８はソース・ドレイン領域、２０９はゲート絶縁膜、２１０は層間絶縁膜、２１１はコンタクト穴、２１２は配線を示す。ＴＦＴ形成の形成方法は第１図の実施例と同様の方法で形成できる。前述のようにＴＦＴのチャンネル領域２１３を結晶粒界の存在する確立がほぼ零の領域に配置することでは結晶粒界による素子特性のばらつきを著減にし、歩留りを大幅に向上させることができた。

非晶質シリコン層のパターン形状は第２図に示した形状の他にも様々な形状が考えられる。例えば、第６図～第８図は本発明の実施例における連結領域の平面図の例を示す。第６図～第８図において、６０１、７０１、８０１はシード領域、６０２、７０２、８０２は島状領域、６０３、７０

3，803は連結領域、604，605，704，705，804，805は結晶粒を示す。連結領域の幅にテーパをつけたり，幅の狭い領域706を設ける等連結領域の形状を工夫することで、結晶成長の選択をより完全に行うことができる。特に、本発明に基づく金属膜を用いたシード形成方法ではシード領域に多結晶核が発生し易いため、上述のような結晶成長の選択が歩留りの大幅な向上に対して有効となる。又、連結領域等にP（リン）等の不純物を10^{19}～$10^{21}cm^{-3}$程度ドープして結晶成長速度を10倍程度に上げることは，熱処理時間の短縮となり，素子形成領域である島状領域をより広く結晶化することができ特に有効である。

尚，第1図～第3図の実施例では金属層としてAlを用いる場合を例としたが，本発明はこれに限定されるものではない。例えば，Al－Si等のAl合金，Cr，Ni，Mo，W，Au，Pt，Ti等の金属もしくはそれらの合金を金属層として用いることもできる。Al－Si等のSiと金属との合金を用いると結晶核が生成し易くなる場合がある。Al－Siの場合を例にとると、Siの含有量を0．5wt%程度以下にすると結晶核が均一に発生し易くなる。（Siの含有量が上述の値より大きくなると，より高温の熱処理を行わないと結晶核が生成し難くなる。）

又，本実施例では非晶質シリコン膜の上に金属層を形成する場合を例としたが，積層順はこの逆でもよい。但し、金属層上に非晶質シリコン層を形成した場合は熱処理時に金属層を除去することができない。金属層の段差部を非晶質シリコン層がステップカバーしなければならない等の制限が生ずる。

又，本発明は，実施例に示したTFT以外にも，絶縁ゲート型半導体素子全般に応用できるほか，バイポーラトランジスタ，静電誘導型トランジスタ，太陽電池・光センサをはじめとする光電変換素子等の半導体素子全般に応用でき，極めて有効な製造方法となる。

（発明の効果）

以上述べたように，本発明によればガラス，石英等の絶縁性非晶質基板，もしくはSiO$_2$等の絶縁性非晶質材料膜等の絶縁性非晶質材料上に単結晶シリコン等を選択的に結晶成長させ，結晶段界が任意する位置を制御できるようになった。その結果，結晶化された領域に選択的に半導体素子を形成することが可能となった。本発明によれば，絶縁性非晶質材料上にSiウェハー上に形成した単結晶素子に匹敵する高性能な半導体素子を形成できるようになった。大型で高解像度の結晶表示パネルや高速で高解像度の密着型イメージセンサや三次元ICをを容易に形成できるようになった。

さらに，溶融再結晶化法とは異なり，本発明はせいぜい650℃程度の低温の熱処理が加わるだけであるため，（1）基板として安価なガラス基板を使用できる。（2）三次元ICでは，下層部の素子に悪影響（例えば，不純物の拡散等）を与えずに上層部に半導体素子を形成することが出来る。等のメリットもある。

また，本発明は，実施例に示したTFT以外にも，絶縁ゲート型半導体素子全般に応用できるほか，バイポーラトランジスタ，静電誘導型トランジスタ，太陽電池・光センサをはじめとする光電変換素子等の半導体素子を絶縁材料上に形成する場合に極めて有効な製造方法となる。

4．図面の簡単な説明

第1図（a）～（d）は本発明の実施例における半導体装置の製造工程図である。

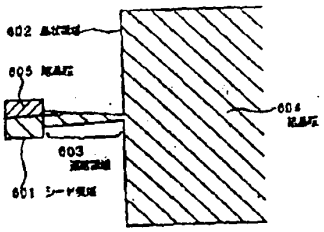
第2図（a）～（d）及び第3図（a）～（d）は本発明の実施例における半導体装置の製造方法であり，第2図は断面図、第3図は平面図である。

第4図及び第5図は結晶成長の模式図である。

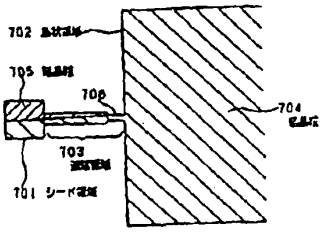
第6図～第8図は本発明の実施例における結晶領域の平面図である。

101，201・・・絶縁性非晶質材料

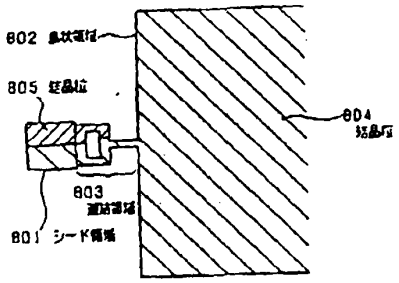
102，202・・・非晶質材料層



第 6 図



第 7 図

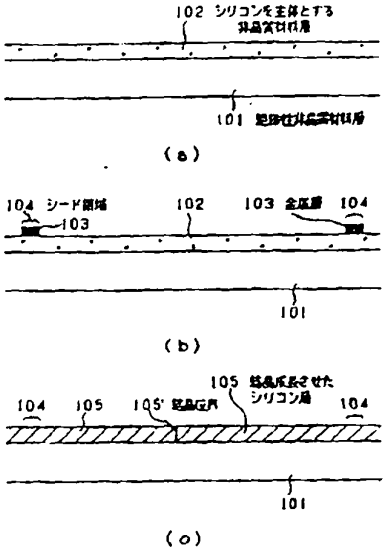


第 8 図

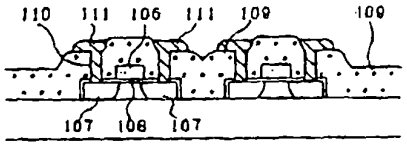
103、203・・・金属層
104、204・・・シード領域
106、207・・・ゲート電極
107、208・・・ソース・ドレイン領域
108、209・・・ゲート絶縁膜
109、210・・・層間絶縁膜
110、211・・・コンタクト穴
111、212・・・配線
401、501、602、702、802
・・・島状領域
402、502、603、703、803
・・・連結領域
403、503、601、701、801
・・・シード領域

以 上

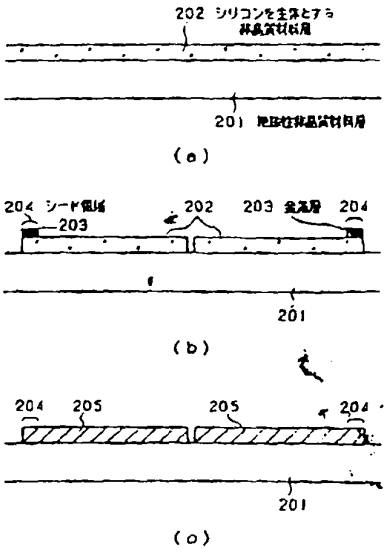
出願人 セイコーエプソン株式会社
代理人 弁理士 上 柳 雅 誉（他1名）



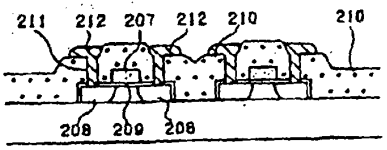
第 1 図



第 1 図

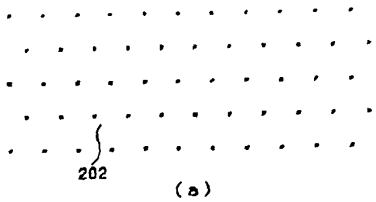


第 2 図

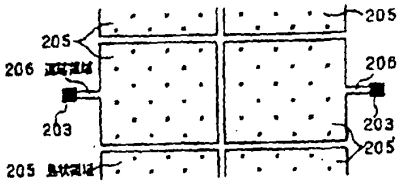


(d)

第 2 図

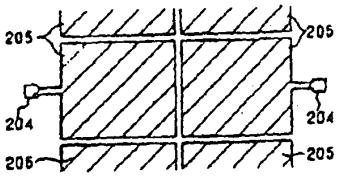


(a)

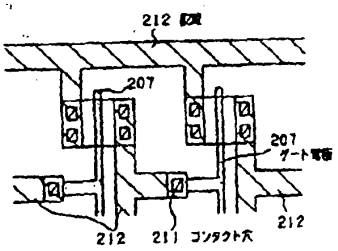


(b)

第 3 図

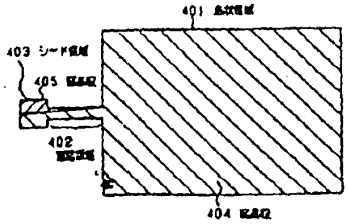


(c)

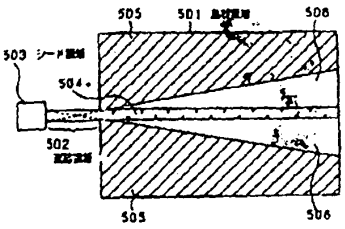


(d)

第 3 図



第 4 図



第 5 図

PTO #96-225

Japanese Kokai Patent
No. Hei 2[1990]-140915

MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICES

Hideaki Oka

UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. OCTOBER 1995
TRANSLATED BY THE RALPH MCELROY TRANSLATION COMPANY

Code: PTO 96-225

JAPANESE PATENT OFFICE

PATENT JOURNAL

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Application No.:	SHO 63[1988]-295065
Application Date:	November 22, 1988
Publication Date:	May 30, 1990
No. of Claims:	1 (Total of 8 pages)
Examination Request:	Not requested

SEMICONDUCTOR DEVICE MANUFACTURING METHOD

[Handotaisochi no seizohoho]

Inventor: Hideaki Oka

Applicant: Seiko Epson Corp.

[There are no amendments to this patent.]

Claim

1. A semiconductor device manufacturing method characterized in that it includes:

(a) a process in which an amorphous material layer which mainly consists of silicon is formed upon insulating amorphous material,

(b) a process in which a metal layer is formed upon the said amorphous material layer for pattern formation,

(c) a process in which crystal nuclei are grown in areas in which the said amorphous material layer makes contact with the said metal layer by heat treatment, for example,

(d) a process in which the said amorphous material layer is crystal grown through a heat treatment, for example, by using the aforementioned crystal nuclei as seeds, and

(e) a process in which a semiconductor element is formed in the silicon layer which is crystal grown.

Detailed explanation of the invention

Field of industrial application

The present invention concerns a manufacturing method for semiconductor devices, in particular, it concerns a manufacturing method for semiconductor devices in which a monocrystalline semiconductor film is selectively formed upon insulating amorphous material.

Conventional technology

Attempts have been made to form a high-performance semiconductor element upon an insulating amorphous substrate, such as glass and quartz, for example, and an insulating amorphous layer, such as SiO_2, for example.

As the need for large, high-definition liquid crystal display panels with high-speed, high-definition contact-type image sensors, and three-dimensional ICs, for example, has increased in recent years, so has the expectation of realizing the aforementioned high-performance semiconductor elements upon an insulating amorphous material.

Using the formation of a thin film transistor (TFT) upon insulating amorphous material as an example, the following is being examined: (1) TFT using amorphous silicon which is formed by the plasma CVD method, for example, as the element material; (2) TFT using polycrystalline silicon which is formed by the CVD method, for example, as the element material; and (3) TFT using monocrystalline silicon which is formed by the fusion recrystallization method, for example, as the element material.

However, of these TFTs, with respect to TFTs using amorphous silicon and polycrystalline silicon as the element materials, the mobility of the carriers with applied electric field of these types of TFTs is dramatically lower than when monocrystalline silicon was used as the element material (amorphous silicon TFT < 1 $cm^2/V \cdot sec$ and monocrystalline silicon TFT ≈ 10 $cm^2/V \cdot sec$), therefore, attainment of a high-performance TFT was difficult.

Also, the fusion recrystallization method using a laser beam, for example, cannot yet be considered a sufficiently developed technology. Moreover, the technical difficulty is particularly great when it is necessary for an element to be formed for a large area as in a liquid crystal display panel, for example.

Therefore, a method in which polycrystalline silicon having a large particle diameter can be solid grown has received much attention and its research has advanced to the point where the technique is an easy yet practical method to form a high-performance semiconductor element on an insulating amorphous material (Thin Solid Films 100 (1983) p. 227, JJAP Vol. 25 No. 2 (1986) p.L121).

Problems to be solved by the present invention

However, sufficient control of the particle diameter of the polycrystalline silicon and the position at which the crystal grain boundary is present was difficult in the conventional technology. Accordingly, even though polycrystalline silicon with a large particle diameter can be tentatively formed, there was a drastic difference between the characteristics of a TFT which is formed with the crystal grain and a TFT with the channel region of the TFT located at the crystal grain boundary. Therefore, serious problems occurred such as the operating speed of scanning circuits constructed from TFT being controlled by the poor characteristics of TFTs located at the crystal grain boundary, and the circuit not operating under worst care conditions, for example.

Therefore, the present invention provides a manufacturing method in which the position of the crystal grain boundary is controlled and a semiconductor element is selectively formed in a crystal region.

Means to solve the problems

The semiconductor device manufacturing method of the present invention is characterized in that it includes:

(a) a process in which an amorphous material layer which mainly consists of silicon is formed upon insulating amorphous material,

(b) a process in which a metal layer is formed upon the said amorphous material layer for pattern formation,

(c) a process in which crystal nuclei are grown in areas at which the said amorphous material layer makes contact with the said metal layer by a heat treatment, for example,

(d) a process in which the said amorphous material layer is crystal grown through a heat treatment, for example, by using the aforementioned crystal nuclei as seeds, and

(e) a process in which semiconductor elements are formed in the silicon layer which is crystal grown.

Application examples

Figure 1 shows one example of manufacturing process diagrams of a semiconductor device in an application example of the present invention. An example in which a thin film transistor (TFT) is formed as a semiconductor element is used in Figure 1.

In Figure 1, (A) indicates a process in which an amorphous material layer (102) which consists mainly of silicon is formed on insulating amorphous material (101), such as an insulating amorphous substrate consisting of glass and quartz, for example, or an insulating amorphous material layer consisting of SiO_2, for example. Methods for forming the said amorphous material layer include forming an amorphous silicon film by plasma CVD, vapor deposition, EB deposition, MBE, sputtering, and CVD, for example; methods in which monocrystalline silicon or polycrystalline silicon, for example, is first formed include plasma CVD, CVD, vapor deposition, EB deposition, MBE, and sputtering, for example, and an element, such as Si, Ar, B, P, He, Ne, Kr, and H, for example, is ion implanted in order to noncrystallize the said monocrystalline silicon or polycrystalline silicon, for example.

(B) indicates a process in which a metal layer (103) is formed upon the said amorphous material layer (102), the said metal layer is eliminated while leaving sections which become seed regions (104), and crystal nuclei which become seeds are formed in areas in which the said amorphous material layer (102) makes contact with the metal layer (103) through heat treatment, for example. Using Al as the metal layer, for example, the temperature of the amorphous silicon which makes contact with the said metal layer (103) is lower than other areas, and crystal nuclei can easily be generated in a short period of time. Accordingly, since heat treatment is processed at the temperature and time at which crystal nuclei are not generated in areas which do make contact with the metal layer, crystal growth can be selectively induced from the seed regions (104). In a specific

example, since heat treatment is processed at approximately 200°C to 450°C for approximately 15 min to 2 h after vapor-depositing Al, for example and pattern forming it, crystal nuclei are formed near the interface between the metal layer and the amorphous silicon layer, and crystal growth starts. The metal layer (Al) (103) is successively removed with phosphoric acid, for example, through etching. The reason for eliminating the metal layer is to prevent an abnormal diffusion of the metal into the amorphous silicon (particularly into the element forming region) during heat treatment at high temperature which successively takes place. The aforementioned abnormal diffusion can also be prevented by establishing the film thickness of the metal layer, such as Al, for example, at least at the same or less than the film thickness of the amorphous silicon layer. For example, the abnormal diffusion can be reduced by using a metal layer of approximately 100-500 Å or less on an amorphous silicon layer of 200-1000 Å.

The heat treatment temperature for forming crystal nuclei has a different optimum value accordingly to the film forming method for amorphous silicon. For example, crystal nuclei are formed at a relatively low temperature of approximately 200-350°C when the amorphous silicon which is formed by the plasma CVD method is used. Accordingly, there is merit in forming crystal nuclei in the seed regions through low temperature heat treatment since it is difficult to generate crystal nuclei in areas other than the seed regions.

(C) indicates a process in which the said amorphous material layer (102) is selectively crystal grown through heat treatment, for example, using the said seed regions (104) as starting

points. The heat treatment temperature is approximately 550-650°C, and heat treatment is applied for approximately 20-30 h.

(D) indicates a process in which a semiconductor element is formed in the crystal grown silicon layer (105). TFT is formed as a semiconductor element in the example in Figure 1 (D). In the figure, (106) is a gate electrode, (107) is a source-drain region, (108) is a gate insulating film, (109) is a layer insulating film, (110) is a contact hole, and (111) is wiring. As one example of the TFT formation method, the silicon layer (105) is patterned and a gate insulating film is formed. The said gate insulating film can be formed by a method using the thermal oxidation method (high temperature process) or by a method at a low temperature of less than 600°C by the CVD method or the plasma CVD method, for example, (low temperature process). Inexpensive glass substrates can be used when the low-temperature process is used, therefore, semiconductor devices, such as large liquid crystal display panels and contact type image sensors, for example, can be fabricated at low cost, and also when forming a three-dimensional IC, for example, a semiconductor element can be formed at the upper layer section without negatively affecting the element at the lower layer section (diffusion of impurities, for example). The gate electrode is successively formed, and the source-drain region is formed by ion injection, thermal diffusion, or plasma doping, for example, and the layer insulating film is formed by the CVD, sputtering, or plasma CVD, for example. Furthermore, a contact hole is formed at the said layer insulating film for forming wiring, and TFT is formed.

The mobility of the carriers with applied electric field of the low temperature processed TFT (n-channel) manufactured by the manufacturing method for semiconductor devices based on the present invention is 200-350 $cm^2/V \cdot sec$, and a high-performance TFT was formed on a glass substrate. This is the result of the selective crystal growth with satisfactory processability by the manufacturing method of the present invention. Furthermore, the defect density is reduced and the aforementioned mobility of the carriers with applied electric field further improves if the process in which the semiconductor element is exposed to a plasma atmosphere formed from a gas, such as hydrogen gas or ammonia gas, is included in the aforementioned TFT forming process.

Figures 2 and 3 indicate another example of manufacturing process diagrams of a semiconductor device in an application example of the present invention. Figure 2 indicates cross-sectional diagrams, and Figure 3 indicates top view diagrams.

In Figures 2 and 3, (A) indicates a process in which an amorphous material layer (202) which consists mainly of silicon is formed on insulating amorphous material (201), such as an insulating amorphous substrate consisting of glass and quartz, for example, or an insulating amorphous material layer consisting of SiO_2, for example. Methods for forming the said amorphous material layer include forming the amorphous silicon by plasma CVD, vapor deposition, EB deposition, MBE, sputtering, and CVD, for example, a method in which monocrystalline silicon or polycrystalline silicon, for example, is first formed by plasma CVD, CVD, vapor deposition, EB deposition, MBE, and sputtering,

for example, and an element, such as Si, Ar, B, P, He, Ne, Kr, and H, for example, is ion implanted in order to noncrystallize the said monocrystalline silicon or polycrystalline silicon, for example.

(B) indicates a process in which a metal layer (203) is formed upon the said amorphous material layer (202), the said metal layer is removed while leaving sections which become seed regions (204), and crystal nuclei which become seeds are formed in an area in which the said amorphous material layer (202) makes contact with the metal layer (203) through heat treatment, for example, and the said amorphous material layer (202) is successively patterned to the desired form. Also, the amorphous material layer can also be patterned before growing the seed regions. Using Al as the metal layer in an example, as described above, the temperature of the amorphous silicon that makes contact with the said metal layer (203) is lower than other areas, and crystal nuclei can easily be generated in a short period of time. Accordingly, since heat treatment is applied at the temperature and time at which crystal nuclei are not generated in areas which do not make contact with the metal layer, crystal growth can be selectively induced from the seed regions. In a specific example, since heat treatment is applied at approximately 200-450°C for approximately 15 min to 2 h, crystal nuclei are formed near the interface between the metal layer and the amorphous silicon layer, and crystal growth starts. The metal layer (Al) (203) is successively removed with phosphoric acid, for example, through etching. As described above, the reason for removing the metal layer is to prevent the abnormal diffusion of the metal into the amorphous silicon

(particularly into the element forming region) during heat treatment at a high temperature which subsequently takes place. The heat treatment temperature for forming crystal nuclei has a different optimum value according to the film forming method for amorphous silicon. For example, crystal nuclei are formed at a relatively low temperature of approximately 200-350°C when the amorphous silicon which is formed by the plasma CVD method is used. Accordingly, there is merit in forming crystal nuclei in the seed regions through a low temperature heat treatment since it is difficult to generate crystal nuclei in areas other than the seed regions.

The amorphous silicon layer is patterned to a specific form. Figure 2 indicates an example in which the aforementioned amorphous silicon layer is patterned to a form which includes island regions (205) and connecting regions (206) which connect the said island region (205) to the said seed region (204).

(C) indicates a process in which the said amorphous material layer (202) is selectively crystal grown through heat treatment, for example, using the said seed regions (204) as starting points. The heat treatment temperature is approximately 550-650°C, and heat treatment is applied for approximately 20-30 h.

By patterning the amorphous silicon layer to include island regions (205) and connecting regions (206) as described above, even when multiple crystal nuclei are formed in the seed regions, any of the connecting regions which are superior (such as a fast crystal growth speed or early generation of crystal nuclei, for example) are selected for fast crystal growth, and the island regions are monocrystallized. Figure 4 indicates a pattern

diagram of the said crystal growth. In Figure 4, (401) is the island region, (402) is the connecting region, (403) is the seed region, and (404) and (405) indicate crystal grains.

As indicated in the pattern diagram of the crystal growth in Figure 5, the location of the existence of the crystal grain boundary can be significantly limited even when monocrystalline growth is not selected in the connecting region. In Figure 5, (501) is the island region, (502) is the connecting region, (503) is the seed region, (504) is a location at which the probability of the existence of the crystal grain boundary is high, and (505) are the areas in which the probability of the presence of the crystal grain boundary is practically zero. (506) is a region between both (gray zone). Accordingly, when using a MOS transistor and TFT as examples of the semiconductor element, a significant variation in element characteristics by the crystal grain boundary can be eliminated by arranging the element so that the channel region of the said element is arranged within the region (405).

(D) indicates a process in which a semiconductor element is formed at the crystal grown island regions (205). TFT is formed as a semiconductor element in the example in Figure 2 (D). In the figure, (207) is a gate electrode, (208) is a source-drain region, (209) is a gate insulating film, (210) is a layer insulating film, (211) is a contact hole, and (212) is wiring. The method of formation of TFT can be the same method as in the application example of Figure 1. As described above, the variation of element characteristics by the crystal grain boundary can be eliminated by arranging the channel region (213) of the TFT in a region at which the probability of the existence

of the crystal grain boundary is practically zero, and the yield significantly improved.

With respect to the pattern of the amorphous silicon layer, various other forms can be considered besides the shapes indicated in Figure 2. For example, Figures 6-8 indicate examples of top view diagrams of connecting regions in the application examples of the present invention. In Figures 6-8, (601), (701), and (801) are seed regions, (602), (702), and (802) are island regions, (603), (703), and (803) are connecting regions, (604) and (605), (704) and (705), and (804) and (805) are crystal grains. The selection of crystal growth can be attained more completely by devising the form of the connecting region, such as by tapering the width of the connecting region and providing a region of narrow width (706), for example. Polycrystal nuclei are easily generated in the seed region particularly in the seed formation method using the metallic film based on the present invention; therefore, the aforementioned selection of the crystal growth effectively brings about a drastic improvement in the yield. Also, the heat treatment time is shortened by increasing crystal growth speed by approximately 10 times by doping with a concentration of approximately $10^{[illegible]}$-$10^{[illegible]}cm^{-3}$ with such impurities as P (phosphorus), for example, in the connecting region, for example, and it is particularly effective when more widely crystallizing the island region, which is the region in which the element is to be formed.

Examples in which Al was used as the metal layer were used in the application examples in Figures 1-3; however, the present invention is not so limited. For example, Al alloys, such as

Al-Si, for example, metals, such as Cr, Ni, Mo, W, Au, Pt, and Ti, for example, and their alloys can be used as the said metal layer. In some cases, crystal nuclei are easily generated when an alloy of Si and a metal, such as Al-Si, for example, is used. Using Al-Si as an example, crystal nuclei are easily and evenly generated when the Si content is less than approximately 0.5 wt% (it is difficult to generate crystal nuclei unless a heat treatment at a higher temperature is applied when the Si content is greater than the aforementioned value).

In the application examples, the metal layer was formed on the amorphous silicon layer; however, the order of lamination can be reversed. However, problems, such as the inability to remove the metal layer before heat treatment and covering areas of the metal layer with step differences with the amorphous silicon layer, for example, occur when the amorphous silicon layer is formed above the metal layer.

Besides the TFTs indicated in the application examples, the present invention can also be applied in general to insulated gate semiconductors, and it can also be applied in general to semiconductor elements such as photoelectronic transducers, bipolar transistors, field-effect transistors, solar batteries, and optical sensors, for example, and it becomes a very effective manufacturing method.

Effects of the present invention

As described above, in the present invention monocrystalline silicon, for example, is selectively grown upon insulating amorphous material, such as an insulating amorphous substrate

consisting of glass and quartz, for example, or an insulating amorphous material layer consisting of SiO_2, for example, and the position at which the crystal grain boundary should be present can be controlled. As a result, it becomes possible to selectively form a semiconductor element in a crystallized region. A high-performance semiconductor element which is equivalent to a semiconductor element that is formed on a Si wafer can be formed on the insulating amorphous material of the present invention, and large, high-definition liquid crystal display panels high-speed high-definition contact type image sensors, and three-dimensional ICs, for example, can be easily formed.

Furthermore, unlike the fusion recrystallization method, low temperature heat treatment, which is approximately 650°C at most, is only auxiliary in the present invention. As a result, there are such merits as (1) the ability to use inexpensive glass substrates as the substrate and (2) the ability to form a semiconductor element at the upper layer section without negatively affecting (diffusion of impurities, for example) the element at the lower layer section in the three-dimensional ICs, for example.

Besides the TFTs indicated in the application examples, the present invention can also be applied in general to insulated gate semiconductors, and it can become a very effective manufacturing method when forming semiconductor elements such as photoelectronic transducers, bipolar transistors; field-effect transistors, solar batteries, and optical sensors, for example, upon the insulating material.

Brief explanation of the figures

Figure 1 (a)-(d) are diagrams indicating manufacturing processes for a semiconductor device in an application example of the present invention.

Figure 2 (a)-(d) and Figure 3 (a)-(d) indicate a manufacturing method for a semiconductor device in an application example of the present invention, Figure 2 indicates cross sectional diagrams, and Figure 3 indicates top views.

Figure 4 and Figure 5 are pattern diagrams of the crystal growth.

Figure 6-8 are top views of the connecting regions in the application examples of the present invention.

101, 201･･･insulating amorphous material, 102, 202･･･amorphous material layer, 103, 203･･･metal layer, 104, 204･･･seed region, 106, 207･･･gate electrode, 107, 208･･･source-drain region, 108, 209･･･gate insulating film, 109, 210･･･layer insulating film, 110, 211･･･contact hole, 111, 212･･･wiring, 401 501, 602, 702, and 802･･･island region, 402, 502, 603, 703, and 803･･･connecting region, and 403, 503, 601, 701, and 801･･･seed region.

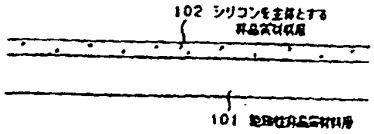

Figure 1 (a)

Key: 101 Insulating amorphous material layer
102 Amorphous material layer mainly consisting of silicon

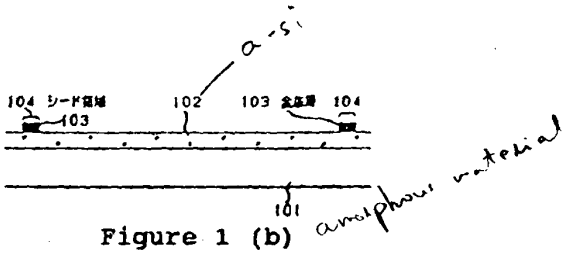

Figure 1 (b)

Key: 103 Metal layer
104 Seed region

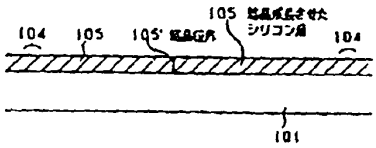

Figure 1 (c)

Key: 105 Crystallized and grown silicon layer
105' Crystal grain boundary

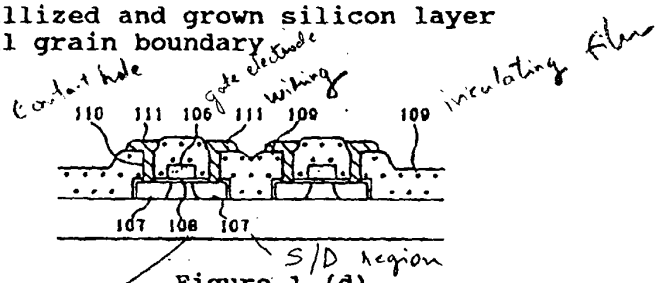

Figure 1 (d)

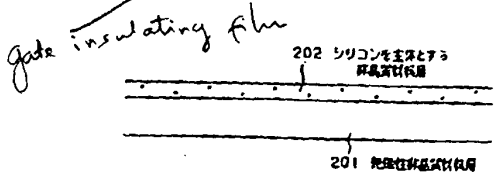

Figure 2 (a)

Key: 201 Insulating amorphous material layer
202 Amorphous material layer mainly consisting of silicon

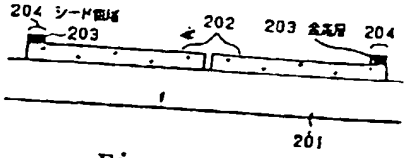

Figure 2 (b)

Key: 203 Metal layer
204 Seed region

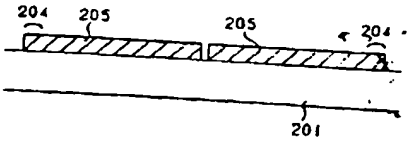

Figure 2 (c)

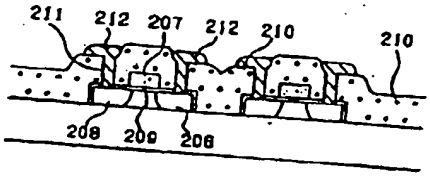

Figure 2 (d)

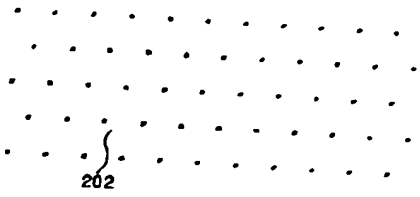

Figure 3 (a)

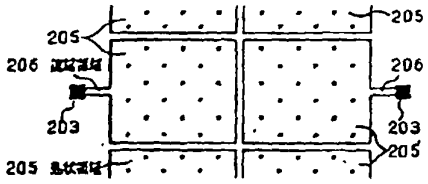

Figure 3 (b)

Key: 205 Island region
206 Connecting region

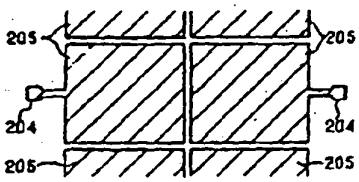

Figure 3 (c)

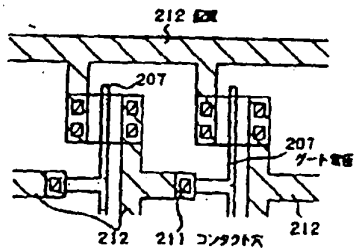

Figure 3 (d)

Key: 207 Gate electrode
211 Contact hole
212 Wiring

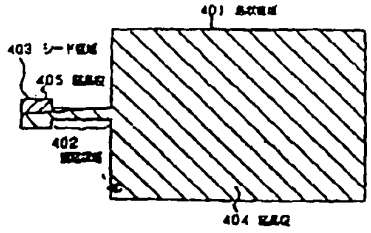

Figure 4

Key: 401 Island region
402 Connecting region
403 Seed region
404 Crystal grain
405 Crystal grain

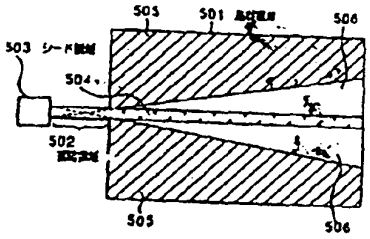

Figure 5

Key: 501 Island region
502 Connecting region
503 Seed region

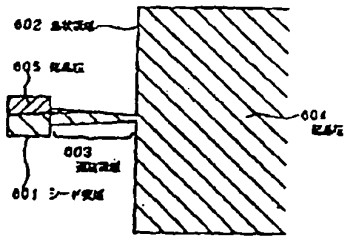

Figure 6

Key: 601 Seed region
602 Island region
603 Connecting region
604 Crystal grain
605 Crystal grain

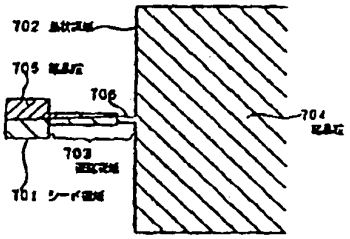

Figure 7

Key: 701 Seed region
702 Island region
703 Connecting region
704 Crystal grain
705 Crystal grain

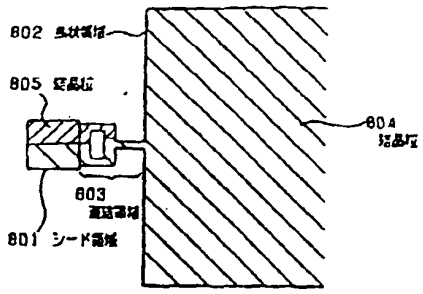

Figure 8

Key: 801 Seed region
802 Island region
803 Connecting region
804 Crystal grain
805 Crystal grain